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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,836	03/09/2004	Gregory W. Starr	ALT-303	5670

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,836	STARR ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-16,19-21 and 24-30* is/are rejected.

7)☒ Claim(s) *6,7,17,18,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1- 30 are presented in the instant application according to the Applicants' filing on 03/09/04.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections

2. Claim 7 is objected to because of the following informalities:

Claim 7, line 2, change "5" to -- 6 -- since it appears to recite limitations depending on claim 6.

Appropriate correction is required.

3. Claims 22 and 23 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claimed limitation is a circuit for outputting a plurality of clock signals that has been described in claim 14, the limitations of the circuit being

comprised in an integrated chip or in a programmable logic device are not considered to further define the claimed invention; as such, claims 22 and 23 are not given patentable weight.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 2, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Caresosa et al. (U.S. Patent No. 6,864,752).

With respect to claim 1, Caresosa et al. discloses, in Fig. 3, a circuit and its corresponding method of concurrently generating a plurality of clock signals derived from a reference signal [refclk_cmu], the method comprising a) receiving the reference signal [refclk_cmu]; b) producing [3] a plurality of signals each having a frequency and a different phase; c) dividing [Div2, Div10, Div17] frequency of each of the produced signals concurrently in accordance with programmable selections of frequency divisors to produce output signals each having a frequency and phase; and d) multiplexing [MUX] the output signals in accordance with

programmable selections such that each clock signal is usable as an off-chip clock signal, an on-chip clock signal, or both *(Note that the limitation "such that each clock signal is usable as an off-chip clock signal, an on-chip clock signal, or both" does not further limit the limitation of claim 1. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus/method from a prior art apparatus/method satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, this limitation has not been given patentable weight).*

With respect to claim 2, Caresosa et al. discloses, in Fig. 3, that the frequency of each of the output signals is different than or the same as one or more of the other of said output signals.

With respect to claim 12, Caresosa et al. discloses, in Fig. 3, a circuit and its corresponding method of providing multiple clock signals based on a reference signal [refclk_cmu], the method comprising a) generating a first plurality of clock signals [3] in response to receiving the reference signal [refclk_cmu]; each of the plurality of clock signals having a different phase; b) generating [Div2, Div10, Div17] concurrently a second plurality of clock signals each having a phase and a selectable frequency; and c) making [MUX] each of the second plurality of clock signals available for a same plurality of clocking applications.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3-5, 11, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caresosa et al. (U.S. Patent No. 6,864,752).

With respect to claim 3, Caresosa et al. discloses, in Fig. 3, a circuit and its corresponding method of concurrently generating a plurality of clock signals including the step of multiplexing [MUX] the output signals. Caresosa et al. does not explicitly disclose multiplexing comprises programmably coupling one of the output signals to an output pin. However, such arrangement of coupling one of the output signals to an output pin has been well known in the art for the output signal at the output pin to be employed in the coupled circuit (see Prior Art of record to Klapproth, US Pat. No. 6,580,288, col. 1, lines 17-33). Therefore, to configure a multiplexing having one of the output signals being coupled to an output pin in the circuit of Caresosa et al. for the stated purpose would have been deemed obvious to an artisan skilled in the art *(For the limitation of "use as an off-chip clock signal" see last paragraph of claim 1 rejection since it is also intended use).*

With respect to claim 4, Caresosa et al. discloses, in Fig. 3, a circuit and its corresponding method of concurrently generating a plurality of clock signals including the step of multiplexing [MUX] the output signals. Caresosa et al. does not explicitly disclose multiplexing comprises programmably coupling one of the output signals to a global clock network. However, such arrangement of coupling one of the output signals to a global clock network has been well known in the art for the output signal to be distributed in the network (see Prior Art of record to New, US Pat. No. 6,720,810, Fig. 2, items 228, 205). Therefore, to configure a multiplexing having one of the output signals being coupled to a global clock network in the circuit of Caresosa et al. for the stated purpose would have been deemed obvious to an artisan skilled in the art.

With respect to claim 5, Caresosa et al. discloses, in Fig. 3, a circuit and its corresponding method of concurrently generating a plurality of clock signals including the step of multiplexing [MUX] the output signals. Caresosa et al. does not explicitly disclose multiplexing comprises programmably coupling one of the output signals to a clock network for use as an on-chip local clock signal. However, such arrangement of coupling one of the output signals to a clock network for use as an on-chip local clock signal to has been well known in the art for the output signal to be distributed in the network in the coupled circuit (see Prior Art of record to Hofer, US Pat. No. 6,665,762, col. 4, lines 19-22). Therefore, to configure a multiplexing having one of the output signals being coupled to a clock network for use as an on-chip local clock signal in the circuit of Caresosa et al. for the stated purpose would have been deemed obvious to an artisan skilled in the art.

With respect to claims 11, 29 and 30, Caresosa et al. discloses, in Fig. 3, a circuit and its corresponding method of converting an input clock signal [refclk_cmu] to a plurality of output clock signals, the method comprising a) modifying [305] the input clock signal having an input frequency to produce a first signal having a first frequency; b) phase-shifting [3] the first signal to produce a plurality of second signals each having a phase and the first frequency, each of the second signals having a phase different than the phase of the others of the second signals; c) modifying [Div2, Div10, Div17] each of the second signals substantially concurrently to produce an output signal having a phase and an output frequency, each of the output signals having an individually selectable output frequency; and d) selectably [MUX]coupling any one of the output signals.

Caresosa et al. does not explicitly disclose multiplexing comprises programmably coupling one of the output signals to a) an output pin, b) a global clock network and c) to a clock network for use as an on-chip local clock signal. However, such arrangements of couplings have been well known in the art depending largely upon the requirements of the application to apply the best suited coupling for performing the particular function (see Prior Art of record to a) Klapproth, US Pat. No. 6,580,288, col. 1, lines 17-33; b) New, US Pat. No. 6,720,810, Fig. 2, items 228, 205; and c) Hofer, US Pat. No. 6,665,762, col. 4, lines 19-22; respectively). Therefore, to configure a multiplexing having one of the output signals to a) an output pin, b) a global clock network and c) to a clock network for use as an on-chip local clock signal in the circuit Caresosa et al. for the stated purpose would have been deemed obvious to an artisan skilled in the art.

8. Claims 8-10, 14-16, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caresosa et al. (U.S. Patent No. 6,864,752) in view of Liang et al. (U.S. Patent No. 5,550,515).

With respect to claim 8, Caresosa et al. discloses a circuit and its corresponding method of providing a plurality of clock signals concurrently, the method comprising the steps of a) programming a plurality of divisors into a respective plurality of frequency dividers [Div 2, Div 10, Div 17], and b) programming at least one multiplexer [MUX] to couple one of a plurality of output signals received from the plurality of frequency dividers to any one of an integrated circuit output pin, a global clock network, or a local clock network.

Caresosa et al. fails to disclose programming a first divisor into a first frequency divider that receives the reference signal.

Liang et al. discloses, in Fig. 2, a first divisor being programmed into a first frequency divider [103] that receives a reference signal [Fpr].

To configure the circuit of Caresosa et al. with a first divisor being programmed into a first frequency divider that receives a reference signal as taught by Liang et al. to acquire the required divided down initial frequency for the synchronization process would have been obvious to one of ordinary skill in the art at the time of the invention since such circuit arrangement of the divider in a phase locked loop for the stated purpose has been a well known practice as evidenced by the teachings of Liang et al. *(see Liang et al., col. 3, lines 40-57).*

With respect to claim 9, the combined teaching of Caresosa et al. and Liang et al. further discloses programming the output of one of plurality of frequency dividers [Div2, Div10, Div17] to be fed into another one of plurality of frequency dividers.

With respect to claim 10, the combined teaching of Caresosa et al. and Liang et al. discloses repeating the programming the output at least once.

With respect to claim 14, Caresosa et al. discloses, in Fig. 3, a circuit comprising a) phase/frequency detector circuitry [305], b) a voltage-controlled oscillator (VCO) [3] coupled to receive the output of said phase/frequency detector circuitry and operative to output a plurality of signals each having a different phase; c) feedback frequency-divider circuitry [Div2, Div10, Div17] coupled to receive the plurality of VCO output signals and operative to output a frequency-divided signal to the second input of the phase/frequency detector; d) first multiplexing circuitry [4:1 MUX] coupled to receive the plurality of VCO output signals and operative to output a plurality of signals selected from the plurality of VCO output signals; and

e) a plurality of frequency dividers [Div2, Div10, Div17] each coupled to the multiplexing circuit to receive one of the output signals from the first multiplexing circuitry and operative to output a frequency-divided signal; and second multiplexing circuitry [MUX]coupled to receive each of the frequency-divided signals from the plurality of frequency dividers, the second multiplexing circuitry operative to programmably output each received frequency-divided signal to any one of a plurality of signal conductors coupled to the second multiplexing circuitry.

Caresosa et al. fails to disclose a first frequency divider operative to receive an input signal.

Liang et al. discloses, in Fig. 2, a first frequency divider [103] that receives a reference input signal [Fpr].

To configure the circuit of Caresosa et al. with a first frequency divider that receives a reference input signal as taught by Liang et al. to acquire the required divided down initial frequency for the synchronization process would have been obvious to one of ordinary skill in the art at the time of the invention since such circuit arrangement of the divider in a phase locked loop for the stated purpose has been a well known practice as evidenced by the teachings of Liang et al. *(see Liang et al., col. 3, lines 40-57).*

With respect to claim 15, the combined teaching of Caresosa et al. and Liang et al. discloses all the claimed limitation in claim 14. Caresosa et al. does not explicitly disclose the signal conductors coupling to one of the output signals to a) an output pin, b) a global clock network and c) to a clock network for use as an on-chip local clock signal. However, such arrangements of couplings have been well known in the art depending largely upon the requirements of the application to apply the best suited coupling for performing the particular

function (see Prior Art of record to a) Klapproth, US Pat. No. 6,580,288, col. 1, lines 17-33; b) New, US Pat. No. 6,720,810, Fig. 2, items 228, 205; and c) Hofer, US Pat. No. 6,665,762, col. 4, lines 19-22; respectively). Therefore, to configure a circuit as taught by Caresosa et al having one of the output signals to a) an output pin, b) a global clock network and c) to a clock network for use as an on-chip local clock signal for the stated purpose would have been deemed obvious to an artisan skilled in the art.

With respect to claim 16, the combined teaching of Caresosa et al. and Liang et al. discloses a third multiplexer circuitry [6:1 MUX] coupled to receive a plurality of input signals and operative to programmably output one of the signals to said first frequency-divider circuitry.

With respect to claim 19, the combined teaching of Caresosa et al. and Liang et al. discloses that the feedback frequency-divider circuitry comprises a multiplexer [6:1 MUX] and a programmable frequency-divider circuit [Div2, Div10, Div 17], the multiplexer coupled to receive the plurality of VCO output signals and operative to output one of the VCO output signals to the frequency-divider circuit, the frequency-divider circuit operative to output a frequency-divided signal to the second input of the phase/frequency detector [305].

With respect to claim 21, the combined teaching of Caresosa et al. and Liang et al. discloses that the circuit is a general purpose phase-locked-loop circuit.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Caresosa et al. (U.S. Patent No. 6,864,752) in view of Liang et al. (U.S. Patent No. 5,550,515), as applied in claim 14, and further in view of Nishimura et al. (U.S. Patent No. 6,542,038).

With respect to claim 20, the combined teaching of Caresosa et al. and Liang et al. discloses all the claimed limitations as expressed in claim 14, except for the circuit being a low voltage differential signaling (LVDS) phase locked loop circuit.

Nishimura et al. discloses, in column 1, lines 38-51, a low voltage differential signaling phase locked loop circuit with compensation of the phase relation between its input and output in relation to the phase offset between the reference signal and the comparison signal.

To configure the circuit of the combined teaching of Caresosa et al. and Liang et al. with the phase locked loop being a low voltage differential signaling phase locked loop for easily detecting phase offset as taught by Nishimura et al. would have been obvious to one of ordinary skill in the art at the time of the invention since Nishimura et al. teaches that such type of phase locked loop would facilitate reliability in reducing the phase offset without increasing phase jitter of the output signal *(see Nishimura et al., col. 1, lines 38-51).*

10. Claim 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caresosa et al. (U.S. Patent No. 6,864,752) in view of Liang et al. (U.S. Patent No. 5,550,515) and further in view of Griesshaber (U.S. Patent No. 5,212,723).

With respect to claims 24-27, the combined teaching of Caresosa et al. and Liang et al. discloses all the claimed limitations as expressed in claim 14, except for the circuit being mounted on a printed circuit board and further a memory and a processor being mounted on the circuit board, and the circuit being coupled to at least one of the processor and the memory.

Grieesshaber discloses, in columns 4-5, lines 53-68, 1-22, respectively, the phase locked loop circuit being mounted on a printed circuit board and further a memory and a processor

being mounted on the circuit board, and the circuit being coupled to at least one of the processor and the memory.

To configure the circuit of the combined teaching of Caresosa et al. and Liang et al. with the phase locked loop being mounted on a printed circuit board with a memory and a processor coupled to at least one of the processor and the memory as taught by Griesshaber would have been obvious to one of ordinary skill in the art at the time of the invention since Griesshaber teaches that such an arrangement would provide the capability of removing ambiguity or aberration in the signals *(see Griesshaber col. 1, lines 38-40).*

11. Claims 13 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Caresosa et al. (U.S. Patent No. 6,864,752) in view of Young (U.S. Patent No. 6,081,141).

With respect to claims 13 and 28, Caresosa et al. discloses all of the claimed limitations as expressly recited in claim 12. Caresosa et al. does not explicitly disclose a) the clocking applications include off-chip clocking, on-chip global clocking, on-chip local clocking, frequency synthesizing, and zero delay buffering, and b) the clocking application circuit being comprised in a programmable logic device in a digital processing system comprising a processor; a memory; a programmable logic device comprising the clocking application circuit, input/output circuitry; a system bus coupling the processor, the memory, the programmable logic device, and the input/output circuitry. However, such clocking applications and of the digital processing system including the clocking application circuit to provide versatility in clocking applications and system synchronization has been taught by New for providing coordination in various part of the circuit system . Therefore, to configure the circuit of Caresosa et al. with all the components as taught by Young for high efficiency in clock coordination and versatility in clocking

applications would have been obvious to one of ordinary skill in the art at the time of the invention since Young teaches that such circuit arrangement would facilitate system synchronization *(see Young, col.17, lines 18-22)*.

Allowable Subject Matter

12. Claim 7 would be allowed if corrected to overcome the objection set forth in this office action.

13. Claims 6-7 (claim 7 is believed to be dependent on claim 6, see Claim Objection) and 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A method of concurrently generating a plurality of clock signals including steps of receiving a plurality of input signals; synchronizing the plurality of input signals with an enable signal; and selecting one of said plurality of input signals to be the reference signal, as called for in claim 6; and

b) A circuit, in which the third multiplexer circuitry comprises a synchronization circuit coupled to receive an enable signal and a selectable two of the plurality of input signals, the synchronization circuit comprising two latches clocked by the enable signal, each latch coupled to receive a respective one of the selectable two signals and operative to output a synchronized signal, as called for in claim 17.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER